EEE 598: Modeling and Design Solutions for Nano-CMOS Technology

T/Th 9:00-10:15am, ECG G224

Instructor

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Office Hours: T/Th 10:30-11:30am, GWC 336

Course Introduction

The advances of CMOS technology have driven the exponential growth of IC design for the past decades. Although many technical problems have been resolved along the way, many new physical challenges emerge as CMOS is scaling into the nanoscale regime. Particular examples include power consumption, process variations, signal integrity, and reliability degradation. In this context, it is critical to seamlessly integrate the physical properties of the underlying silicon with IC design solutions, in order to continue along the path predicted by Moore's law.

This course discusses advanced compact modeling, circuit design techniques, and EDA tools for sub-65nm CMOS technology. The first part of the course covers physical principles and operational characteristics of short-channel MOSFET transistors. Based on the SPICE model, emphasis is on the behavior of MOSFET dictated by present and probable future technologies. Particular modeling topics include short-channel and high field effects, various leakage mechanisms, device modeling for circuit simulations, as well as variability and reliability. Modeling and design for SOI and multi-gate transistors will be further explored. The comprehensive understanding of transistors will provide a solid ground to analysis and design for nano-CMOS technology. In the rest of the course, we will look at solutions in practice to overcome emerging design hurdles. Examples will be drawn from the essence of high-performance microprocessor design, with special topics on low-power design, robust design under variations, and statistical design and analysis. Industrial lecturers will be invited to present the state-of-art practices, while fundamental principles will be reinforced by literature survey.

The learned knowledge and related circuit simulation tools will be practiced in assignments. The research project will be developed to integrate the understanding of nanoscale technology and leading design challenges.

Prerequisites

This course requires basic understanding of CMOS operation and integrated circuits design. Knowledge and design capability comparable to EEE 525 are required.

Suggested Reading

- *Design of High-Performance Microprocessor Circuits*, Edited by Anantha Chandrakasan, William J. Bowhill, and Frank Fox.
- *Nano-CMOS Circuit and Physical Design*, by Ban P. Wong, Anurag Mittal, Yu Cao, and Greg Starr.
- *MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4*, by William Liu.

Grading Policy

Homeworks (3):	15%
Project (2 students/team, white paper + midterm report + presentation + final paper): 5% + 10% + 25% + 15%	
Final Exam (take-home):	30%

A+	10%
A	> (average + 0.5σ)
A-	> average
B+:	> (average - 0.5σ)
B:	> (average - σ)
B-:	> (average -1.5σ)
C:	else