Ongoing research into wireless transceivers in the 60 GHz band is required to address the demand for high data rate communications systems at a frequency where signal propagation is challenging even over short ranges. This thesis proposes a mixer architecture in Complementary Metal Oxide Semiconductor (CMOS) technology that uses a voltage controlled oscillator (VCO) operating at a fractional multiple of the desired output signal. The proposed topology is different from conventional subharmonic mixing in that the oscillator phase generation circuitry usually required for such a circuit is unnecessary.

Analysis and simulations are performed on the proposed mixer circuit in an IBM 90 nm RF process on a 1.2 V supply. A typical RF transmitter
system is considered in determining the block requirements needed for the mixer to meet the IEEE 802.11ad 60 GHz Draft Physical Layer Specification. The proposed circuit has a conversion loss of 21 dB at 60 GHz with a 5 dBm LO power at 20 GHz. Input-referred third-order intercept point (IIP3) is 2.93 dBm. The gain and linearity of the proposed mixer are sufficient for Orthogonal Frequency Division Multiplexing (OFDM) modulation at 60 GHz with a transmitted data rate of over 4 Gbps.